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DESIGNING DIGITAL CONTROLLERS FOR A CONTROLLED PLANT

Abstract: This paper report contains an explanation of how to design a digital controller using the Laplace Transform to z-Transform conversion method. The objectives are that the controlled system should track step input with a reasonably small steady-state error and a settling time faster than the open-loop settling time. Furthermore, it should do so with the minimum overshoot that is reasonably possible. The main contribution is to establish the feasibility and ease of the systematic design procedure and future work will focus in more detail on applying the Sampling Theorem and deadbeat controller.

There are several objectives that the controlled system should reach:

1. Track step input with a reasonably small steady-state error and a settling time which should be faster than the open-loop settling time.
2. Gain a small overshoot that is sufficiently possible.
3. Have a systematic design procedure.

A method for finding the parameters of the deadbeat controller in the MatLab environment is presented. Based on the results obtained the simulation reveals that even when the control grows by one-step, the settling time of the system response could be less than that of the deadbeat controller. The work shows that deadbeat could be a powerful analysis tool since it is possible to grab the entire dynamic easily using several samples.

Keywords: z-transform, Sampling Theorem, deadbeat.

Introduction

The target is to digitalize the system 1, designing the digital controller using the Sampling Theorem. Moreover, there is required to have full explanation of selecting the sampling period.

$$G(s) = \frac{1}{s(s + 0.3)(s + 22)(s + 100)} \quad (\text{system 1})$$

Furthermore, it is needed to design a deadbeat controller for system 2. Finally, there should be explained the quantization effect on the system.

$$G(s) = \frac{1}{s(s+10)(s+50)} \quad (\text{system 2})$$

Part 1. Sampling Theorem

For the system shown in eq. 1 there should be performed the digitalization.

$$G(s) = \frac{1}{s(s+0.3)(s+22)(s+100)} \quad (1)$$

a. Let us consider the requirements of having overshoot PO less than 15% and the steady-state error $e_{ss} \leq 0.04$. In this case, there is performed a phase-lead controller using the Bode method [1].

$$e_{ss} = \frac{1}{K_v} \Rightarrow K_v = \frac{1}{e_{ss}} = \frac{1}{0.04} = 25 \quad (2)$$

Because the value of K must be adjusted so that it would meet the basic specifications of having the velocity error constant $K_v \geq 25$ and percentage overshoot $PO \leq 15\%$, there should be applied Equation 3:

$$K_v = \lim_{s \rightarrow 0} s \frac{K}{s(s+0.3)(s+22)(s+100)} = 2 \quad (3)$$

$$\frac{K}{(0.3) * (22) * (100)} = 25$$

$$K = 16500$$

The damping ratio ξ of the system is: $\xi = -\frac{\ln \frac{PO}{100}}{\sqrt{\ln \frac{PO}{100} + \pi^2}} = 0.7797$.

By using the value of the damping ratio ξ there could be found the desired phase margin PM_d (see eq. 4):

$$\begin{aligned} PM_d = \phi_m &= \tan^{-1} \frac{2\xi}{\sqrt{-2\xi^2 + \sqrt{1 + 4\xi^4}}} \\ &= \tan^{-1} \frac{2*0.7797}{\sqrt{-2*0.7797^2 + \sqrt{1 + 4*0.7797^4}}} = 69^\circ \end{aligned} \quad (4)$$

Next, there could be obtained the gain crossover frequency ω_{gc} which is the frequency at which the gain $20 \log |G(j\omega_{gc})| = 0 \text{ dB}$ (see eq. 5-6).

$$\left| \frac{16500}{j\omega_{gc}(j\omega_{gc}+0.3)(j\omega_{gc}+22)(j\omega_{gc}+100)} \right| = 1 \quad (5)$$

By changing $t = \omega_{gc}^2$, it yields to:

$$\begin{aligned} t^4 + 10484.09t^3 + 4840943.56t^2 + 435600t - 272250000 &= 0 \\ t \approx 7.3957 \Rightarrow \omega_{gc} &\approx 2.7195 \end{aligned} \quad (6)$$

Subsequently, the actual phase margin for our uncompensated system [2] could be defined as follows (see eq. 7):

$$PM = 180^\circ + \angle G(j\omega_{gc}) = 180 - 90 - \tan^{-1} \frac{\omega_{gc}}{0.3} - \tan^{-1} \frac{\omega_{gc}}{22} - \tan^{-1} \frac{\omega_{gc}}{100} \approx -2.3095^\circ \quad (7)$$

Finally, it makes it possible to find the phase lead including a 10% safety factor for the compensator as it is shown in eq. 8:

$$\Phi(\omega_m) = PM_d + 0.1 * PM_d - PM = 78.2071^\circ \quad (8)$$

The evaluation of the value of α could be found by using the formula shown below:

$$\sin \Phi(\omega_m) = \frac{\alpha-1}{\alpha+1} \quad \Rightarrow \quad \alpha \approx 93.7545 \quad (9) [6]$$

The frequency at which the maximum phase lead happens is (see eq. 10-11):

$$20 \log |G(j\omega_{gc})| = -10 \log \alpha \quad (10)$$

This yields to:

$$\frac{1}{\alpha} = \frac{16500^2}{\omega_m^2(\omega_m^2+0.3^2)(\omega_m^2+22^2)(\omega_m^2+100^2)} \quad (11)$$

By finding ω_m , it is accepted as a new gain crossover frequency ω'_{gc} :

$$\omega_m = \omega'_{gc} \approx 8.2305 \quad (12)$$

Therefore, compensator poles and zeros are evaluated (13 and 14 respectively):

$$\omega_m = \frac{p}{\sqrt{\alpha}} \quad \Rightarrow \quad p = \omega_m \sqrt{\alpha} = 8.2305 * 9.6827 \approx 79.6939 \quad (13)$$

$$z = \frac{p}{\alpha} = \frac{79.6939}{93.7545} = 0.85 \quad (14)$$

Last, there should be found new gain (see eq. 15) [8]:

$$K_{new} = \alpha * K \approx 93.7545 * 16500 \approx 1546949 \quad (15)$$

The compensated system obtained from these calculations is (see eq. 16 and fig. 1):

$$G_c(s)G(s) = 1546949 \frac{(s+0.85)}{(s+79.6939)} * \frac{1}{s(s+0.3)(s+22)(s+100)} \quad (16)$$

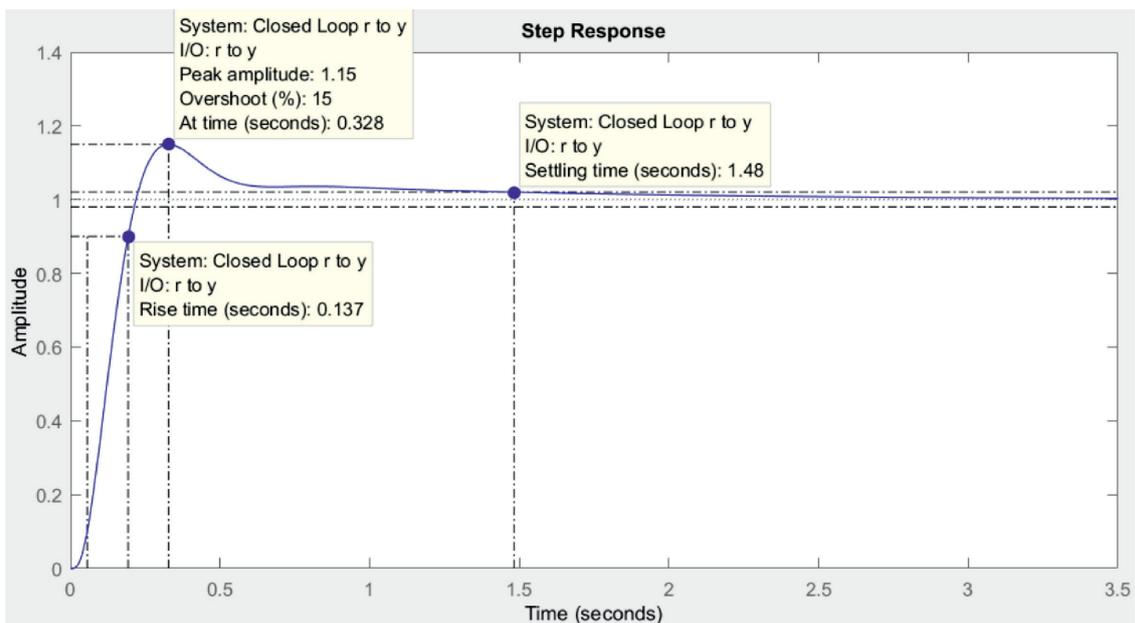


Fig.1. Step Response.

Digital Control

In order to define the system in the digital domain, there should be selected the sampling period T_s by which the system could be sampled. For a good initial estimate of the order of magnitude of the sampling period to start doing some analysis, there could be used a Thumb Rule (see eq. 17):

$$T_s \approx \frac{1}{10B} \quad (17)$$

where B is a bandwidth of our closed-loop system. The bandwidth is found by measuring the frequency when the closed-loop frequency response has declined 3dB from its low-frequency value as it is illustrated in Fig.2.

This yields to find the initial sampling period using the rule of thumb (see eq. 18):

$$T_s \approx \frac{1}{10 \cdot 2.39} \approx 10^{-2} \quad (18)$$

Subsequently, the system is digitized as follows (see eq. 19-20):

$$G_c(s) = 1546949 \frac{(s+0.85)}{(s+79.6939)} \Rightarrow G_c(z) = 1546949 \frac{(z-e^{-0.85 \cdot 0.01})}{(z-e^{-79.6939 \cdot 0.01})} = 1546949 \frac{(z-0.9941)}{(z-0.4507)} \quad (19)$$

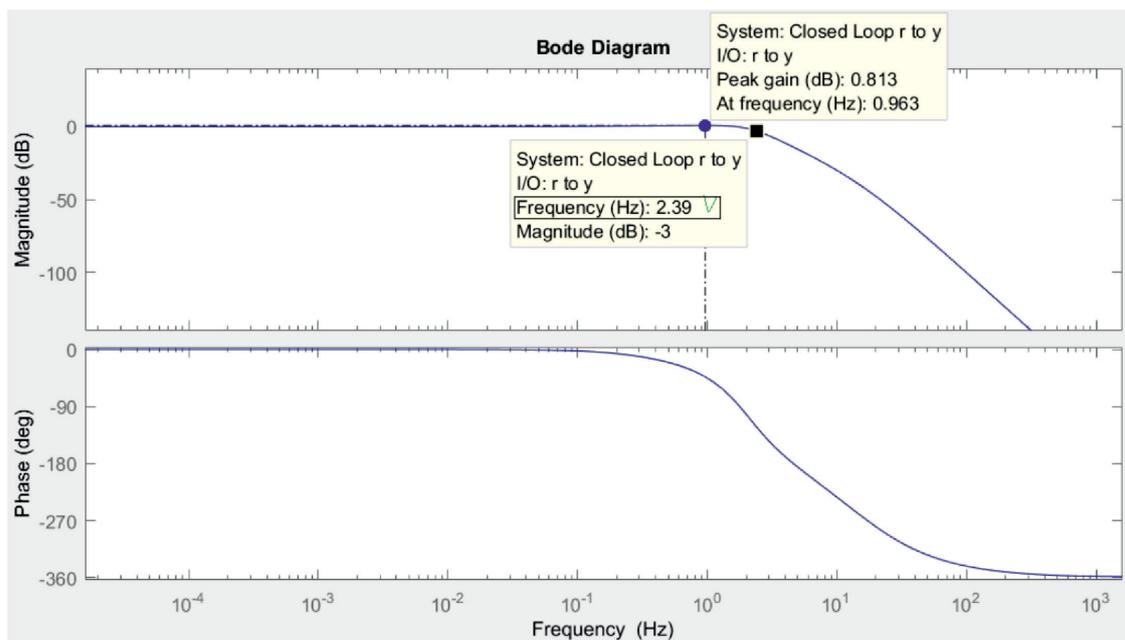


Fig. 2. Bode diagram of closed-loop system.

$$G(s) = \frac{1}{s(s+0.3)(s+22)(s+100)} \Rightarrow G(z) \quad (20)$$

$$= \frac{3.3016 \cdot 10^{-10} (z+7.9240)(z+0.0773)(z+0.7850)}{(z-1)(z-0.9970)(z-0.8025)(z-0.3679)}$$

To perform this task there was created a MatLab program (see Fig.3):

```

1 - close all; clear all;
2 - syms s;
3 - % Plant system
4 - eq1 = expand(s*(s+0.3)*(s+22)*(s+100));
5 - expression_coefficients1 = sym2poly(eq1);
6 - Gs = tf(1,expression_coefficients1);
7 - % Controller
8 - Gc = 1546949*tf([1,0.85],[1,79.6939]);
9 - % Closed-loop of compensated system
10 - GSCCL = feedback(Gc*Gs, 1);
11 - % Sampling period
12 - Ts = 0.01;
13 - % Digitalization
14 - Gz = c2d(Gs, Ts, 'zoh');
15 - Gcz = c2d(Gc, Ts, 'zoh');
16 - % Closed-loop of compensated system in digital domain
17 - GZCCL = feedback(Gz*Gcz, 1);
18 - step(GSCCL,GZCCL)
19 - legend('Analog domain','Digital')
20
21 %% Distortion
22 - T_axis=0:Ts:1;
23 - y_analog=step(GSCCL,T_axis);
24 - hold
25 - y_digital=step(GZCCL,T_axis);
26 - figure
27 - stem(T_axis,(y_analog-y_digital).^2)
28 - MSE=norm(y_analog-y_digital)/length(T_axis)

```

Fig.3. Matlab program.

Finally, the system in both analog domain and the digital domain will look as it is demonstrated in Fig.4 and their distortion is shown in Fig.5.

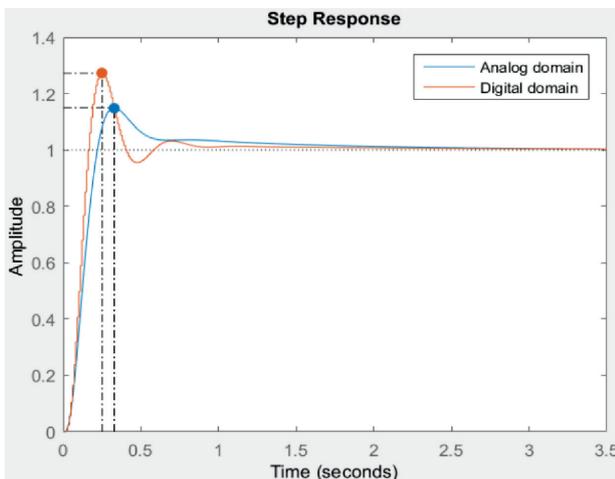


Fig. 4. Step response

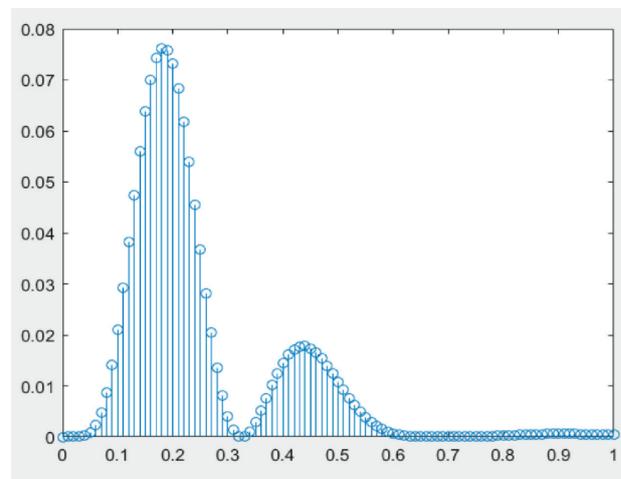


Fig. 5. Distortion

Nevertheless, as it could be seen from the graphs, the digitalized system is not the same as it used to be in analog domain. This kind of mismatches extremely changes the original signal

so that digital to analog conversion will give us not accurate results which means that the sampling period which was taken by thumb rule was not completely correct [10].

Generally, the sampling frequency ω_s should be as big enough as there would be no overlaps between the periodic repetitions of the spectrum, which means that half of it should be more than $2\pi B$, because otherwise, it would cause an aliasing (see eq. 21):

$$\begin{aligned} \frac{\omega_s}{2} > 2\pi B &\Rightarrow \frac{\omega_s}{2\pi} > 2B \\ f_s > 2B &\Rightarrow T_s < 2B \end{aligned} \quad (21)$$

Another important point is that ADC and DAC converters sometimes could not perform their tasks when sampling time is too small, which leads to increase of computational complexity. Moreover, sampling at very small sampling periods introduces numerical errors. [3] Finally, by analyzing the system behavior, it was come to decision to take sampling time $T_s = 0.0016$.

Subsequently, the system is digitized as follows (see eq. 22-23):

$$G_c(s) = 1546949 \frac{(s + 0.85)}{(s + 79.6939)} \Rightarrow \quad (22)$$

$$G_c(z) = 1546949 \frac{(z - e^{-0.85 \cdot 0.0016})}{(z - e^{-79.6939 \cdot 0.0016})} = 1546949 \frac{(z - 0.9987)}{(z - 0.8803)}$$

$$G(s) = \frac{1}{s(s + 0.3)(s + 22)(s + 100)} \Rightarrow \quad (23)$$

$$G(z) = \frac{2.6267 \cdot 10^{-13} (z + 9.5246)(z + 0.0971)(z + 0.9616)}{(z - 1)(z - 0.9995)(z - 0.9654)(z - 0.8521)}$$

Finally, the system in both analog domain and the digital domain will look as it is demonstrated in Fig.6 and their distortion is shown in Fig.7.

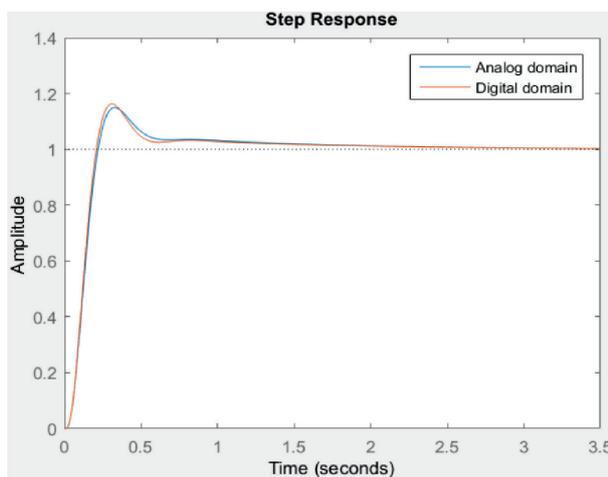


Fig. 6. Step response.

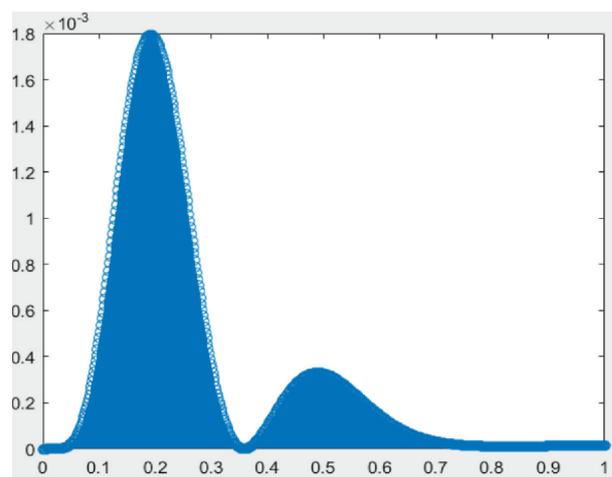


Fig. 7. Distortion.

b. As it could be seen from Fig.6, the final digitalized system is approximately the same as the system in analog domain. If we take a look on its distortion in Fig.7 the highest difference, which is seen in 0.1-0.3 sec. time range, is $1.8 \cdot 10^{-3}$. Another mismatch effect could be seen in this distortion fluctuation in 0.4-0.6 time period, with the maximum point of $0.3 \cdot 10^{-3}$. Nevertheless, these values are too small to say that they could make significant change on our initial signal, because they are approximately zero.

Table 1. System parameters

Quantity	Value
Steady state error to a unit ramp	0.025
Rise Time	0.137
Settling Time	1.48
Percentage Overshoot	15%
Phase Margin	55.1 deg
Gain Margin	15.6 dB
Bandwidth	2.39 Hz

Part 2. Deadbeat controller

For the system shown in eq. 1 there should be designed a deadbeat digital controller.

$$G(s) = \frac{0.01}{s(s+10)(s+50)} \quad (1)$$

a. First, there should be found the given system in the digital domain. But in order to perform the digitalization, there should be chosen a sampling period T_s . In deadbeat digital control, the sampling period is the only design parameter and the settling time directly depends on it. Thus, if T_s is selected to be very small, then it means that the settling time will be very small as well. Furthermore, the sampling period could also have an impact on the magnitude of the control signal. It is observed that system (1) is starting to oscillate from $T_s < 0.133948$.

Other boundaries that are explored in designing a deadbeat digital controller that it is for Stable and Minimum Phase Systems, and for Stable and Non-Minimum Phase Systems. Thus, as it is known that in Stable and Minimum Phase Systems all zeros of numerator and denominator should be inside the unit circle, it is decided to select sampling period to be $T_s = 0.22$. So the system in the digital domain will be as follows (see eq. 2):

$$G(s) = \frac{0.01}{s(s+10)(s+50)} \Rightarrow G(z) = \frac{2.277 \cdot 10^{-6}(z+0.7065)(z+0.0069)}{(z-0.9999999)(z-0.1108)(z-1.6702 \cdot 10^{-5})} \quad (2)$$

Consequently, as all zeros of numerator and denominator are inside the unit circle, the deadbeat digital controller will be as it is shown in eq. 3:

$$D(z) = \frac{A[z]}{z^{-d}B[z]} \frac{z^{-d}}{1-z^{-d}} \Rightarrow D(z) = \frac{4.3917 \cdot 10^5 (z-0.9999999)(z-0.1108)(z-1.6702 \cdot 10^{-5})}{(z+0.7065)(z-1)(z+0.0069)} \quad (3)$$

The final response of this system in digital domain is demonstrated in figures 1-2.

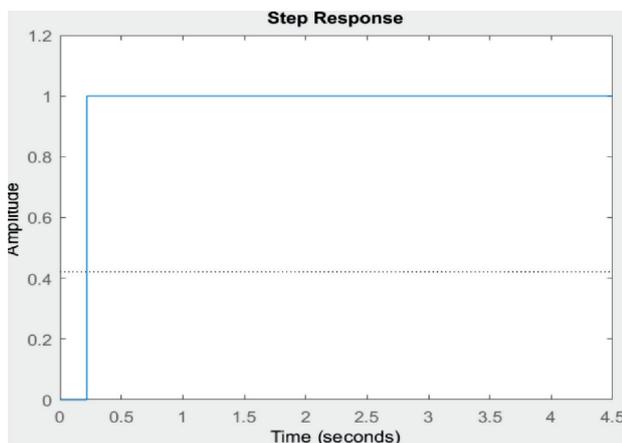


Fig. 1. Output Response.

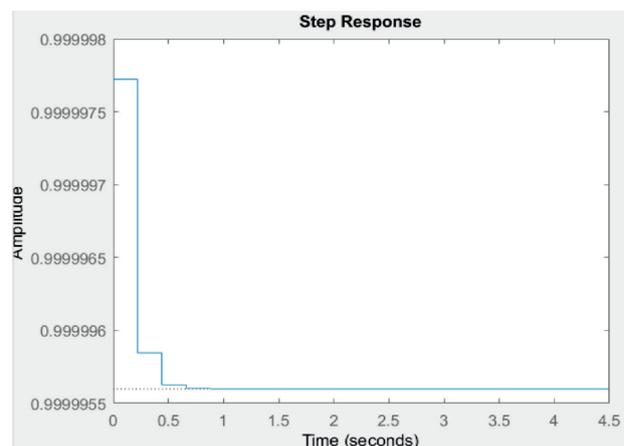


Fig. 2. Control Response.

```

1 - close all; clear all;
2 - syms s;
3 - % Plant system
4 - eq1 = expand(s*(s+10)*(s+50));
5 - expression_coefficients1 = sym2poly(eq1);
6 - Gs = tf(0.01,expression_coefficients1);
7 - % Closed-loop of compensated system
8 - GSCCL = feedback(Gs, 1);
9 - % Sampling period
10 - Ts = 0.22;
11 - % Digitalization
12 - Gz = c2d(Gs, Ts, 'zoh');
13 - z = zp('z', Ts);
14 - % Deadbeat digital controller
15 - Gcz = (1/Gz)*((z^(-1))/(1-z^(-1)));
16 - % Closed-loop of compensated system in digital domain
17 - GZCCL = feedback(Gz*Gcz, 1);
18 - % Closed-loop of deadbeat digital controller
19 - GDCCL = feedback(Gcz, 1);
20 - step(GZCCL)
21
22 - figure
23 - step(GDCCL)
    
```

Fig. 3. Matlab Program.

b. The quantization process should start from finding the uniform quantizer step size Δ . For this there should be chosen the quantity of bits to work with for quantizing, for instance, let us assume that we need 3-bit quantizer. Subsequently, there could be found the Δ (see eq. 4) [4]

$$\Delta = \frac{R}{2^{b+1}} = \frac{1}{2^3} = 0.125 \quad (4)$$

The digitalized (sampled) plant system is as follows (see eq. 5 and Fig.4):

$$T_s = \frac{1}{10B} = \frac{1}{10 \cdot 2 \cdot 10^{-5}} \approx 5000 \quad (5)$$

$$G(z) = \frac{0.1 z^2 + 2.4 \cdot 10^{-6} z}{z^3 - z^2}$$

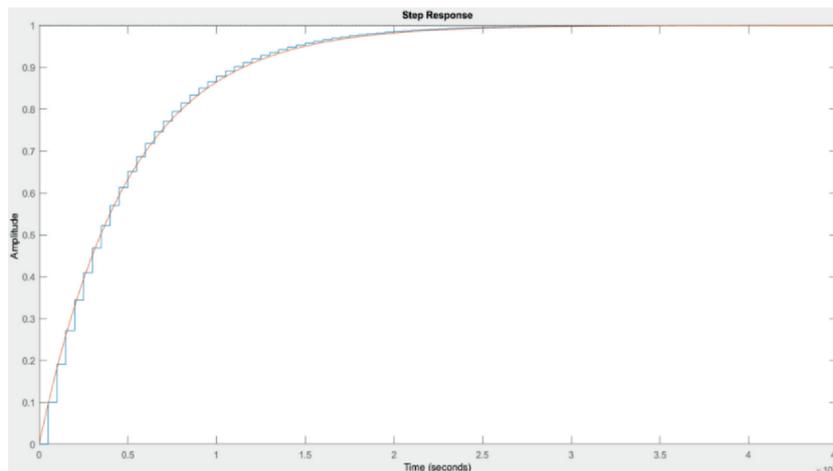


Fig. 4. Sampled system.

Then, by the basic principle of quantization the sampled $x[n]$ could be quantized as it is illustrated in Fig.4:

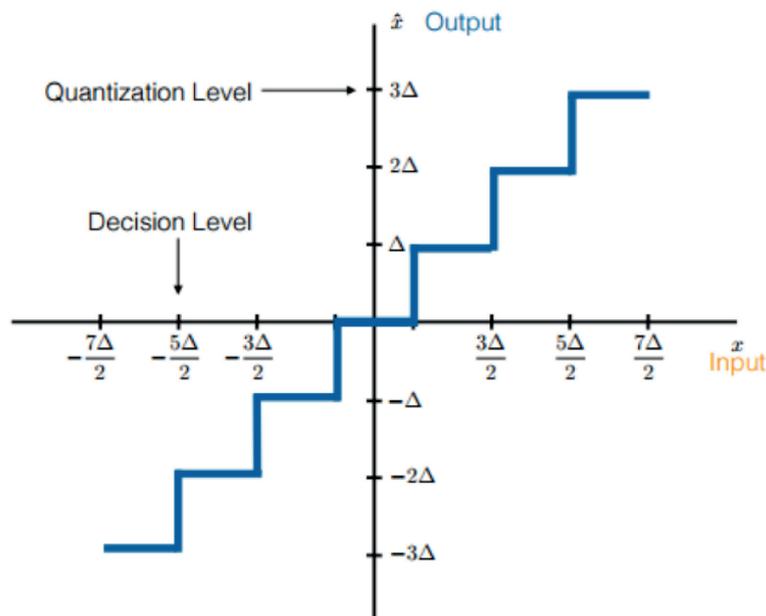


Fig. 5. Quantization rule. [5]

Finally, there could be retrieved a quantized system $x_q[n]$ (see Fig.6).

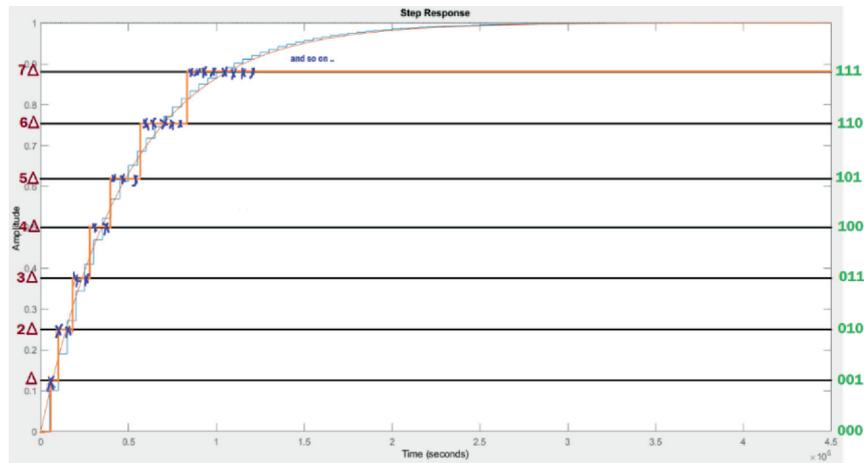


Fig. 6. Quantization of system.

Nevertheless, it has quantization error (quantization noise) which depends on how much bits there used to quantize the signal (see eq. 6) [5]. As it could be seen from the Fig.6, the quantization in 3 bits has upper boundary of 7Δ .

$$|e_q(n)| = |x_q(n) - x(n)| \leq \frac{\Delta}{2} \quad (6)$$

Conclusion

Taking everything into consideration it could be concluded that the digitalization process by ADC converter has great opportunities in converting the system from analog to digital domain. Significance in choosing sampling time is crucial since ADC and DAC converters usually fail

to perform their tasks when dealing with oversampling and under sampling, it could lead to increase of computational complexity or introduce numerical errors. In this article, all experiments were made using Sampling Theorem and systematic modeling of the deadbeat controller.

Results are revealing that the digital controller can perfectly match our needs to be about the same as in analogue domain when a reasonable sampling period is used. In analogue controllers, cost increases with complexity because of increasing number of control loops.

Moreover, executing control in continuous time can be too sensitive than doing so in discrete – time which could lead to poor performance when it faces abrupt noises.

The work in this paper is at its initial stage and in future studies; we desire to look more carefully at problems like working under constraints and noises.

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